Docket No. 740116-358

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Confirmation No. 4774
Heinz WALTER et al.	:	Group Art Unit: 2857
Application No. 10/051,297	:	Examiner: Jeffrey R. West
Filed: January 22, 2002	:	
For: ELECTRICAL TRANSDUCER	:	

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following is submitted in furtherance of the appeal proceedings instituted by a Notice of Appeal filed January 11, 2008, in response to the final Office Action mailed October 11, 2007, in connection with the above-captioned patent application.

I. Real Party in Interest

The assignee, i f m electronic gmbh of Teichstrasse 4, 45127 Essen, Germany, is the real party in interest.

II. Related Appeals and Interferences

There are no related appeals or interferences.

III. Status of the Claims:

Claims 1, 4-17, 20 and 21 are currently pending, all other claims having been canceled. All of these claims have been rejected and the rejection of all of these claims has been appealed.

IV. Status of Amendments:

Amendments to claims 4 and 21 were filed on March 6, 2008, in accordance with 37 C.F.R. §§ 1.116 and 41.33(a), and are reflected in the claims contained in the Claims Appendix of this Brief. No decision as to entry of these amendments had been made at that time of filing of this Brief; however, for purposes of this appeal, entry of the above amendments to claims 4 and 21 is in order, since they merely obviate the claim objections made in the final Office Action without raising any new issues requiring further consideration and/or search and since they merely correct typographical informalities.

V. Summary of Claimed Subject Matter:

Claim 1 is directed to an electrical transducer 1 (Figs. 1 & 7) using a two-wire process, that has an analog sensor 2 that detects a quantity to be measured, and an analog end stage 3 connected downstream of the sensor 2 at the output end of the transducer 1. The transducer 1 has a processor circuit 4 that is not connected serially between the sensor 2 and the analog end stage 3, so that a separate analog measurement signal transmission path is realized, the analog end stage 3 converting an output signal of the sensor 2 into an impressed output current with a magnitude which is a measure of the quantity to be measured (paragraph [0035], lines 1-11, page 11) and is fixed in the range of 0 to 20 mA (page 2, paragraph [0003], lines 1-3). The electronic transducer 1 is controlled by the processor circuit 4 so that, during normal operation of the electrical transducer 1, the processor circuit 4 is shifted temporarily from an awake mode into a sleep mode in which the processor circuit 4 is inactive (pages 11-12, paragraph [0036], lines 1-13). The analog measurement signal transmission path includes an analog scaling unit 8 and the output signal U_p of the sensor 2 and at least one analog setting value , U_1, U_3, U_S are supplied to analog scaling unit 8, and the output signal U_4 of the analog scaling unit 8 is supplied to the analog end stage 3. The output signal U_p of the sensor 2 is routed past the processor circuit 4 via the analog signal transmission path when the processor 4 is in the sleep mode for enabling changes in the quantity being measured to be followed while the processor circuit 4 is inactive page 6, paragraph [0013], lines 1-8), wherein the processor circuit 4 has an activity time in which the processor circuit is active which is shorter than the time that the processor circuit 4 remains in

the sleep mode (page 5, paragraph [0011], lines 1-9). The analog scaling unit 8 includes an analog arithmetic circuit 10. The at least one analog setting value U_1, U_3, U_S is a DC voltage signal or a direct current signal which is delivered to the analog arithmetic circuit 10 of the analog scaling unit 8, wherein at least one active integrator 9 is connected to the processor circuit 4 and to the analog scaling unit 8 as an actuator for producing the DC voltage signal or direct current signal U_1, U_3, U_S (pages 12-13, paragraph [0039], lines 1-12).

Dependent claim 14 adds to the features of claim 1 that three power supply terminals 22-24 are provided, one of which is connected to a detector means 28 so that the transducer automatically switches to three-wire operation when a predetermined power supply voltage is applied to that power supply terminal, (Fig. 6b; page 18, paragraph [0054], lines 1-4).

Dependent claim 15 adds to the features of claim 14 that the detector means 28 is connected to the processor circuit 4, and the processor circuit 4 permanently shifts into the awake mode during the three-wire operation of claim 14 (Fig. 6b; pages 18 and 19, paragraph [0054], lines 4-10).

Independent claim 16 recites a method of producing an indication of a measured value uses an electrical transducer 1, as described above, to produce an output current which is proportional to the measured value so that an analog measurement signal transmission path is realized. In accordance with the method, the electronic circuit (the analog end stage 3) converts an output signal of the sensor 2 into an impressed output current with a level corresponding to the measured value, the electrical transducer 1 being programmed using the processor circuit 4 so that, during normal operation of the transducer, the processor circuit 4 is shifted temporarily into a sleep mode, the output signal of the sensor 2 being supplied to an analog scaling unit 8, and at least one analog setting value U_1, U_3, being supplied to the analog scaling unit 8, and the output signal of the analog scaling unit 8 being supplied to the electronic circuit (analog end stage 3).

No means plus function recitations in accordance with 35 USC § 112, paragraph 6, are present in the claims.

In addition, the invention includes recognition that, with the invention, "[i]f the **activity time of the processor circuit**, i.e., the time during which the processor circuit is not in the sleep mode, but **in the awake mode, is much shorter than** the time in which the processor circuit remains in **the sleep mode**, the **power consumption** of the processor circuit **can be limited** by the selected measure on the average **to a fraction of the nonstop consumption**," (paragraph [0012], lines 5-8, page 5).

Those claims, the substance of which is not described above are considered to rise or fall with the claim(s) from which they depend.

VI. Grounds of Rejection to be Reviewed on Appeal

Claims 1, 4, 5, 7, 9, 16, 17, 20, and 21 stand rejected under 35 U.S.C. § 103 as being unpatentable over Popp, D. E. Patent No. 4016922, when viewed in combination with Zyl, U.S. Patent No. 5,416,723 and Yasui et al., U.S. Patent No. 5,886,565.

Claims 14 and 15 stand rejected under 35 U.S.C. § 103 as being unpatentable over Popp, Zyl, and Yasui et al., when viewed in combination with Brennan et al. U.S. Patent No. 5,252,967.

The following rejections need only be considered to the extent that they implicitly apply to the claims from which the claims rejected on these grounds depend:

Claim 6 stands rejected under 35 U.S.C. § 103 as being unpatentable over Popp, Zyl, and Yasui et al., when viewed in combination with Bruccoleri et al. U.S. Patent No. 5,714,903.

Claim 8 stands rejected under 35 U.S.C. § 103 as being unpatentable over Popp, Zyl, Yasui et al., and Bruccoleri et al., when viewed in combination with Henson, U.S. Patent No. 3,805,092.

Claim 10 stands rejected under 35 U.S.C. § 103 as being unpatentable over Popp, Zyl, and Yasui et al., when viewed in combination with Takamuki, U.S. Patent No. 6,057,794.

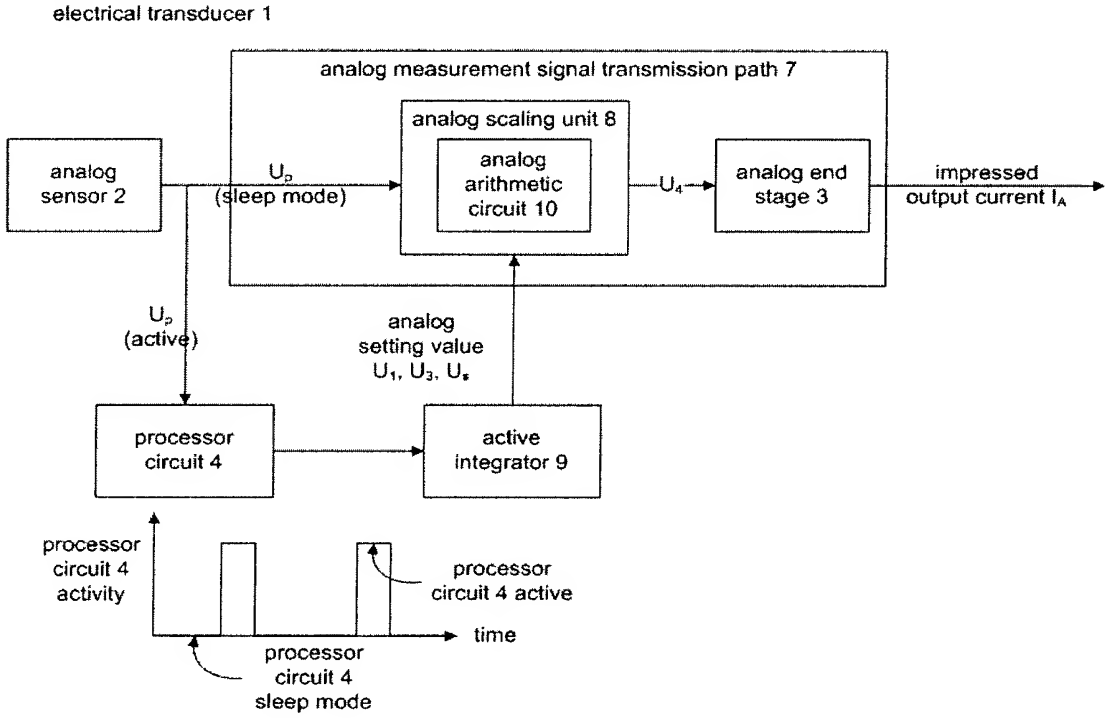
Claims 11-13 stand rejected under 35 U.S.C. § 103 as being unpatentable over Popp, Zyl, and Yasui et al., when viewed in combination with Haynes, U.S. Patent No. 5,207,101.

VII. Argument

Rejection of Claims 1, 4, 5, 7, 9, 16, 17, 20, and 21 under 35 U.S.C. § 103 as being unpatentable over Popp, when viewed in combination with Zyl, and Yasui et al.

Independent claims 1 and 16 and claims dependent therefrom are allowable over Popp, Zyl, Yasui et al., Bruccoleri et al., Henson, Takamuki, Haynes, and Brennan et al., because Popp, Zyl, Yasui et al., Bruccoleri et al., Henson, Takamuki, Haynes, and Brennan et al. fail to render obvious the invention recited in the claims which have been rejected on the basis thereof for the following reasons.

For example, independent claims 1 and 16 include the novel and unobvious feature of a processor circuit having **an activity time** in which the processor circuit is active **which is shorter than** the time that the processor circuit remains in **a sleep mode**, and as illustrated in the figure below.



Advantageously, "the **power consumption** of the processor circuit **can be limited** ... on the average **to a fraction of the nonstop consumption**," (paragraph [0012], lines 5-8, page 5).

Thus, the invention of claims 1 16 includes the novel and unobvious feature of a processor circuit having an activity time in which the processor circuit is active which is shorter than the time that the processor circuit remains in a sleep mode.

By contrast, Popp is directed an electrical transducer with a processor circuit 7 **operated at a low clock frequency**, in order to reduce the power consumption of the processor circuit 7, the purpose of which is only to perform corrective interventions.. Popp does **not** disclose, teach or suggest that the processor circuit 7 is inactive during normal measurement operation, and therefore, also does not teach that the processor circuit 7 should be shifted into a sleep mode at such times. Specifically, Popp only discloses that dynamic output signals 2, 3, 4 of the sensor 1 are routed past the processor circuit 7 via an analog signal transmission path comprising circuits 1, 6, 12 and 13, and that the processor circuit 7 never interferes with the analog signal transmission path. This, however, does not teach that the processor circuit 7 is inactive during the time that the processor circuit 7 is not carrying out corrective interventions on the analog transmission path.

Specifically, in column 1, lines 52-56, Popp discloses that the processor circuit 7 also exchanges digital data via the circuit 13 with an **external** communication unit. Accordingly, the fact that the processor circuit 7 carries out only corrective interventions on the analog transmission path, does teach or suggest that the processor circuit 7 is inactive at any time, much less having an activity time in which the processor 7 is active and which is shorter than the time that the processor 7 remains in a sleep mode, as required by the recitations of independent claims 1 and 16.

Accordingly, it is submitted that the Examiner has misinterpreted the Popp disclosure, particularly with respect to at least the claimed sleep mode. As noted above, Popp is silent with respect to shifting a processor into sleep mode at any time. Specifically, in paragraph 4 of the English translation of the Popp reference, Popp states that the processor circuit 7 carries out corrective **interventions** on the analog transmission path. However, even when the processor circuit 7 does not carry out such corrective interventions on the analog transmission, the processor circuit 7 **must** still be active. Otherwise, if the processor circuit 7 were in a sleep mode, the A/D converters 8, 10 and 5.1-5.3 coupled to the processor circuit 7 and needed for such corrective interventions would also be inactive, so that corrective

interventions in the analog transmission path would not be possible during such a sleep mode. Moreover, in the transducer of Popp, there is no need to shift the processor circuit 7 into a sleep mode, because due to the low clock rate of the processor circuit 7, power consumption is already reduced.

Therefore, the Examiner's characterization, at page 5, second paragraph, of the Final Office Action, that the invention of Popp does teach a microprocessor that is not active during normal operation, but only active to perform corrections is clearly erroneous, and is based on an incorrect interpretation of what is disclosed by Popp.

For example, as can be seen from Fig. 1 of Popp, the sensor 1 determines measured values dp, P and T and **at the same time** converts these parameters into corresponding analog signals 3-4, of which the analog signal 2 (corresponding to the differential pressure dp) is fed to a first input of the combinatorial circuit 6, and to the input of the analog/digital converter 5.3. Since **these values are measured continuously** by the sensor 1, there does not exist a time when the measurements "have been completed" as is clear from paragraph 003 of the English translation of Popp, where it is stated:

> The invention is based on the objective of developing a measuring transducer of the initially cited type, the **continuously delivered output signal of which** is also able to follow rapid changes of the parameter to be measured **without interruption**.

Accordingly, if the processor circuit 7 were to be shifted into a sleep mode, it would be impossible for the processor circuit 7 to exchange digital data with the external communication unit, because there would not be any data signals from the processor circuit 7 at the second input of the transducer interface 13.

Likewise, if the processor circuit 7 were to be shifted temporarily into a sleep mode, the analog/digital converters 5.1, 5.2 and 5.3 connected upstream, and the analog/digital converters 8 and 10 connected downstream of the processor circuit 7 would not be active, and therefore the combinatorial circuit 6 would not be able to combine the analog signal 2 corresponding to the difference pressure dp with the first and second analog correction signals 3 and 4 corresponding to P and T.

Accordingly, Popp fails to disclose, teach or suggest, the invention of independent claims 1 and 16, including the novel feature of a processor circuit having an activity time in

which the processor circuit is active which is shorter than the time that the processor circuit remains in a sleep mode, nor any advantages thereof.

Zyl fails to cure the noted deficiencies of Popp, and thus, fails to render obvious the features recited in the claims for the following reasons.

Zyl is directed to a two-wire electrical transducer including an analog sensor that detects a quantity to be measured, an analog end stage, and a microprocessor, wherein the microprocessor is connected **serially** between the sensor (piezoelectric transducer 10) and the analog end stage 16. While Zyl does disclose **two alternative manners** for achieving low power consumption, but both manners are **only used when** a deficit in the ability of a power regulating circuit to meet the requirements of the microprocessor is detected. Accordingly, if there is no deficit, the microprocessor is **not** shifted into a sleep mode. Therefore, during normal operation of the transducer of Zyl, the microprocessor is not shifted into sleep mode.

In addition, Zyl does not suggest combining his two alternative manners for achieving low power consumption, because it is satisfactory to use one of the two techniques and no reason for using both techniques is suggested, or even indicated to be feasible. Specifically, if the microprocessor is operated with a low clock frequency, the power consumption is reduced and there is no need to shift the microprocessor into a sleep mode.

In Zyl, a sensing circuit is configured to signal a deficit in the capability of the power regulating circuit to supply the combined power requirements of the microprocessor and measuring circuit elements. Zyl provides a means to control the microprocessor in response to the signaling by the sensing circuit of such a deficit, so as to delay further execution of programs by the microprocessor to sufficiently reduce the combined power requirements. Specifically, in column 3, lines 52-56 and column 4, lines 37 – 42, Zyl states:

> When the **microprocessor is operating normally**, the line P is monitored regularly to determine whether the microprocessor should execute an instruction putting the microprocessor into "sleep" mode.
>
> During operation of the transducer with the **microprocessor operating in its normal mode**, the microprocessor and its associated circuits, other than that of Q5, will draw a comparatively steady current which will depend largely on the clock rate of the microprocessor.

Therefore, during normal operation of the electrical transducer of Zyl, the microprocessor is **active** and the power consumption is monitored. Only if the power consumption is too high, does Zyl employ one of the two alternative manners for achieving low power consumption. One technique, as noted above, is analogous to that of Popp, in that the clock rate of the processor is reduced. In the other technique, the microprocessor is shifted into a sleep mode, which results in **halting** of program execution and of **measurement processes** controlled by the microprocessor. This can be clearly seen from the description, at column 2, lines 20-30, and from claim 1 of Zyl.

In both of Zyl's alternatives, initiation of power reduction or the sleep mode is triggered by the occurrence of a power deficit. Accordingly, the microprocessor is shifted into a sleep mode **only if there is a power deficit**. However, when the microprocessor is shifted into the sleep mode, the electrical transducer can not operate to follow any changes in the quantity being measured by the sensor because of reliance on the microprocessor for such measurements. This is evidenced in column 5, lines 26-31, of Zyle which states:

> **...the microprocessor must remain fully operative during "real time" operations** such as the generation of a shot or pulse of acoustic energy, and sampling, analog to digital conversion and storage of the return echo signal, also subsequent processing may safely be discontinuous. (Emphasis added.)

Accordingly, in Zyl, the microprocessor circuit is not shifted temporarily into a sleep mode during **normal operation**, as required by claims 1 and 16, but does so only in the case of a power deficit, and when the microprocessor is operated at a low clock frequency, the processor will **not** be shifted into a sleep mode, due to the low current consumption.

Therefore, because the processor circuit 7 of Popp is operated at **a low clock frequency**, there is no need to shift the processor circuit 7 temporarily into a sleep mode, as taught by Zyl since it is already operating using Zyl's alternative power conservation technique. Finally, because Zyl's shifting of the microprocessor temporarily into a sleep mode results in halting of program execution and hence of measurement process, the microprocessor circuit Popp cannot be temporarily shifted into a sleep mode during normal operation, as required by claims 1 and 16, and still perform as intended.

Nonetheless, even if it proper to combine the teaching of Popp and Zyl, the resulting device would be an electrical transducer having an analog measurement signal transmission

path and a digital signal transmission path, which includes the processor, wherein the processor is operated at a low clock frequency during normal operation, with the processor would be shifted into a sleep mode **only if there is a power deficit**.

With regard to the Examiner's response to Appellants' previous arguments, at pages 12-19 of the Final Office Action, none of the Examiner's arguments address the above facts that clearly show that any combination of the Popp and Zyl references that is made in a manner consistent with their teachings would not lead one of ordinary skill to the Appellants' claimed invention, since Popp requires continuous sensing and output, while Zyl does not teaches implementation of a sleep mode during such "real time" operations.

Accordingly, Popp and Zyl, alone or in combination, fail to render obvious a processor circuit having an activity time in which the processor circuit is active which is shorter than the time that the processor circuit remains in a sleep mode, as required by claims 1 and 16.

Yasui et al. fails to cure the noted deficiencies in the teachings of the Popp and Zyl references. Specifically, Yasui et al. do not disclose, teach or suggest a processor circuit having an activity time in which the processor circuit is active which is shorter than the time that the processor circuit remains in a sleep mode, as required by claims 1 and 16. Moreover, Yasui et al. do not disclose, teach or suggest an electrical transducer or an analog arithmetic circuit or an active integrator as an actuator for a DC voltage signal or a direct current signal, as required by claims 1 and 16. In contrast, Yasui et al. disclose a reference voltage generating circuit for generating a stable reference voltage with low power consumption, and which voltage is suitable for use in an integrated circuit. The reference voltage generating circuit includes a voltage divider formed by resistors R11, R12, and a low-pass filter formed of the resistor R12 and a capacitor C. Furthermore, the reference voltage generating circuit of Yasui et al. is not disclosed as being connected to a processor circuit and to a scaling unit, as required by claims 1 and 16.

Accordingly, claims 1 and 16 cannot be rendered obvious by anything that can be derived from the Popp, Zyl and Yasui et al. references, whether taken alone or in combination.

Claims 14 and 15 stand rejected under 35 U.S.C. § 103 as being unpatentable over Popp, Zyl, and Yasui et al., when viewed in combination with Brennan et al. U.S. Patent No. 5,252,967.

Brennan et al. also fails to cure the above noted deficiencies of the Popp, Zyl and Yasui et al. references. Furthermore, with respect to this rejection, as argued in a previous response, Brennan et al. does not disclose an electrical transducer having three power supply terminals 22-24, one of which is connected to a detector means 28 so that when a predetermined power supply voltage is applied to that power supply terminal, the transducer automatically switches from two-wire to three-wire operation as recited in claim 14, or wherein the detector means 28 is connected to the processor circuit 4, and the processor circuit 4 shifts permanently into the awake mode during three-wire operation as in claim 15.

To the contrary, Brennan et al. discloses a two-wire/three-wire utility data communications system for remotely reading utility meter registers using a hand-held reading unit. Therefore, if this reference is compared with the subject matter of the present patent application, the claimed electrical transducer must be compared with the electric meter 47 and not with the reader/programmer 1.

As can be seen from Fig. 8 of Brennan et al., the reader/programmer 1 comprises a two-wire input/output circuitry 67 and a three-wire/fourteen wire input/output circuitry 69, which are both connected with a microprocessor 64. Additionally, the reader/programmer 1 comprises a battery 79 which supplies DC power to microprocessor 64, two wire I/O circuit 67, three-wire/fourteen wire I/O circuit 69 and other related circuitry of reader/programmer 1. Therefore, Brennan et al.'s reader/programmer 1 comprises at least five outputs and **always** two power supply terminals connected to the battery 79.

Because the known reader/programmer 1 comprises a battery, a detector means for the power supply voltage that is applied to one of the power supply terminals is unnecessary. Brennan et al.'s reader/programmer 1 can be used in both two-wire inductive coupling and three-wire metallic coupling modes, as can be seen from column 3, lines 15–30, where it is stated that:

> Thus, the utility meter data communication system of the present invention is adaptable for operation in both two-wire and three-wire modes. Preferably, when operating in the two-

> wire mode, the remote reader/programmer and encoder are inductively coupled....
>
> When in the three-wire mode, the remote reader/programmer and encoder are directly, electrically coupled over at least three-wires with the first-wire carrying clock signals generated by the reader/programmer, a second line carrying data signals from the encoder and a third line constituting electrical ground.

The way that the known reader/programmer 1 is shifted from the two-wire mode to the three-wire mode is described in column 19, lines 41- 59 as:

> Upon contact of sensor switch 85 with the surface of the button-like inductive port 7 of two wire local network 43 shown in Fig. 1, the closure of switch 85 indicates to the two wire I/O circuitry 67 that probe/adapter 9 is in contact with two wire port 7.
>
> The closure of sensor switch 85 causes two wire 110 circuitry 67 and microprocessor 64 to be activated for the purpose of either reading or programming any encoded registers connected to the two wire local network 43. It should be noted that reader/programmer 1 may further include a manual trigger 87 (see Figs. 1 and 8) which is a normally-open switch that can be used to manually activate the two wire or three/fourteen wire I/O circuits 67 and 69 and microprocessor 64."

Therefore, beside the fact, that Brennan does not disclose the noted features, the known reader/programmer 1 operates in the two-wire mode depending of the state of a touch-sensitive switch 85 or a manual trigger 87 and **not** when a predetermined power supply voltage is applied to a power supply terminal, as required by claims 14 and 15.

As a result Brennan et al. does not and cannot disclose or suggest the features of claims 14 and 15. That is, nothing in Brennan et al.'s disclosure could teach having one of three power supply terminals connected to a detector means so that, when a predetermined power supply voltage is applied to the connected one of the power supply terminals, the transducer automatically switches to three-wire operation as recited in claim 14, and the same is true for having the detector means connected to the processor circuit so as to cause the processor circuit to permanently shift into the awake mode during three-wire operation as recited in claim 15.

Accordingly, claims 14 and 15 are not obvious from Popp, Zyl and Yasui et al., even when combined with Brennan et al.

Rejections of Claims 6, 8, and 10-13 under 35 U.S.C. § 103 as being unpatentable over Popp, Zyl, and Yasui et al., when viewed in combination with Bruccoleri et al., Henson, Takamuki, or Haynes.

To the extent that these rejections implicitly apply to the claims from which they depend, it is noted with respect to the Bruccoleri et al., Henson, Takamuki, and Haynes references, which have been cited with respect to features of these dependent claims that have been indicated to rise or fall with their parent claim, that none of these references contain disclosures which would cure the indicated deficiencies of the Popp, Zyl and Yasui et al. references with respect to claims 1 and 16, nor has the Examiner contended that they any of these references disclose the features argued by Appellant to be unsuggested by the Popp, Zyl and Yasui et al. references. Accordingly, claims 1 and 16 are allowable over all of the applied references, alone or in combination.

Conclusion

On the basis of the foregoing, all of the Examiner's rejections should be reversed and such action is hereby requested.

The brief fee set forth in 37 CFR § 41. 20(b)(2) is authorized to be charged to the Deposit Account No. 50-2478(740116-358) of the undersigned's firm in a separate paper that accompanies this Brief. However, should that paper be missing, this paragraph should be construed as containing such an authorization.

Respectfully submitted,

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VIII. Claims Appendix

1. (Previously Presented) An electrical transducer using a two-wire process comprising:

an analog sensor that detects a quantity to be measured;

an analog end stage which is connected downstream of the sensor at the output end of the transducer;

a processor circuit; and

wherein the processor circuit is not connected serially between the sensor and the analog end stage so that a separate analog measurement signal transmission path is realized, the analog end stage converting an output signal of the sensor into an impressed output current with a magnitude which is a measure of the quantity to be measured and is fixed within a range of about 0 to 20 mA, the electrical transducer being controlled by the processor circuit, wherein during normal operation of the electrical transducer, the processor circuit is shifted temporarily from an awake mode into a sleep mode in which the processor circuit is inactive, the analog measurement signal transmission path including an analog scaling unit, the output signal of the sensor and at least one analog setting value are supplied to the analog scaling unit, and the output signal of the analog scaling unit is supplied to the analog end stage; wherein the output signal of the sensor is routed past the processor circuit via the analog signal transmission path when the processor is in said sleep mode for enabling changes in the quantity being measured to be followed while the processor circuit is inactive;

wherein the processor circuit has an activity time in which the processor circuit is active which is shorter than the time that the processor circuit remains in the sleep mode; wherein the analog scaling unit comprises analog arithmetic circuit; wherein said at least one analog setting value is a DC voltage signal or a direct current signal which is delivered to the analog arithmetic circuit of the analog scaling unit; and wherein at least one active integrator is connected to the processor circuit and to the analog scaling unit as an actuator for producing said DC voltage signal or direct current signal.

2-3. (Cancelled).

4. (Currently amended) The electrical transducer of claim [[3]] 1, wherein the at least one active integrator is a component of a control circuit within the processor circuit.

5. (Previously Presented) The electrical transducer of claim 1, wherein the analog arithmetic circuit comprises at least one analog multiplier.

6. (Original) The electrical transducer of claim 5, wherein the analog multiplier is a single quadrant multiplier.

7. (Previously presented) The electrical transducer of claim 5, wherein the analog arithmetic circuit further comprises at least one subtractor and at least one adder.

8. (Original) The electrical transducer of claim 5, wherein the analog arithmetic circuit comprises a plurality of transistors and a plurality of operational amplifiers.

9. (Original) The electrical transducer of claim 1, further comprising a power source that produces a non-zero output current.

10. (Previously presented) The electrical transducer of claim 6, wherein an adder is connected to the input of a single quadrant multiplier, and a subtractor and an adder are connected to the output of the single quadrant multiplier.

11. (Previously presented) The electrical transducer of claim 1, further comprising an attenuator, having an adjustable time constant, connected between the analog scaling unit and the analog end stage.

12. (Previously presented) The electrical transducer of claim 11, wherein the attenuator comprises a plurality of different RC elements which are selectively connectable via the processor circuit.

13. (Previously presented) The electrical transducer of claim 11, wherein an analog error at the output of the attenuator is compensated by a control circuit.

14. (Previously presented) The electrical transducer of claim 1, further comprising three power supply terminals, one of which is connected to a detector means so that when a predetermined power supply voltage is applied to said one of the power supply terminals, the transducer automatically switches to three-wire operation.

15. (Original) The electrical transducer of claim 14, wherein the detector means is connected to the processor circuit, and the processor circuit shifts permanently into the awake mode during three-wire operation.

16. (Previously Presented) A method of producing an indication of a measured value with an electrical transducer via an output current which is proportional to the measured value, the transducer comprising a sensor, an analog end stage which is connected downstream of the sensor at the output end of the transducer, an electronic circuit which is connected downstream of the sensor, and a processor circuit which is not connected serially between the sensor and the analog end stage so that an analog measurement signal transmission path is realized, the electronic circuit converting an output signal of the sensor into an impressed output current with a level corresponding to the measured value and is fixed within a range of about 0 to 20 mA, the electrical transducer being programmed using the processor circuit, wherein during normal operation of the transducer, the processor circuit is shifted temporarily from an awake mode into a sleep mode in which the processor is inactive, the output signal of the sensor is supplied to an analog scaling unit, at least one analog setting value is supplied to the analog scaling unit, and the output signal of the analog scaling unit is supplied to the electronic circuit; wherein the output signal of the sensor is routed past the processor circuit via the analog signal transmission path when the processor is in said sleep mode for enabling changes in the quantity being measured to be followed while the processor circuit is inactive;

wherein the processor circuit has an activity time in which the processor circuit is active which is shorter than the time that the processor circuit remains in the sleep mode;

wherein the analog scaling unit comprises analog arithmetic circuit;

wherein said at least one analog setting value is a DC voltage signal or a direct current signal which is delivered to the analog arithmetic circuit of the analog scaling unit; and

wherein at least one active integrator is connected to the processor circuit and to the analog scaling unit as an actuator for producing said DC voltage signal or direct current signal.

17. (Previously Presented) The electrical transducer of claim 1, wherein at least one active integrator, as an actuator for at least one direct current signal, is connected to the processor circuit and to the analog scaling unit.

18-19. (Cancelled).

20. (Previously Presented) The electrical transducer of claim 1, wherein the impressed output current is fixed within a range of about 4 to 20 mA.

21. (Currently amended) The ~~electrical transducer~~ method of claim 16, wherein the impressed output current is fixed within a range of about 4 to 20 mA.

IX. Evidence Appendix

None

X. Related Proceedings Appendix

None